



Utkaarsh Gupta

Analog Design • Analog Layout • Hubballi, Karnataka, India

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SUMMARY

Final-year ECE student (CGPA 8.98) focused on analog IC design and analog layout. Led a four-member team through a transistor-level synchronous buck converter in UMC 180 nm (paper submitted to NKCON), and drew DRC- and LVS-clean standard cells and a two-stage op-amp layout in Cadence Virtuoso.

EDUCATION

KLE Technological University

B.E. Electronics and Communication Engineering; CGPA: 8.98

Hubballi, Karnataka

Oct 2023 – Jun 2027

Impulse PU Science College

Pre-University Course (PUC): 82%

Hubballi, Karnataka

Jun 2023

Dk Public School

Secondary School (Class X): 78.2%

Hubballi, Karnataka

Jun 2021

TECHNICAL SKILLS

Analog: CMOS analog design, analog layout, op-amp design, DC–DC converters, loop compensation, DRC/LVS

EDA Tools: Cadence Virtuoso (Schematic, ADE, Layout XL), Spectre, Cadence Allegro, LTspice, Proteus, MATLAB/Simulink

Programming: C, Embedded C, Verilog

Embedded: STM32, ARM, Arduino, ESP32

Coursework: IC packaging in Cadence Allegro (wire-bond, flip-chip, BGA), Analog Electronics, Network Theory

PROJECTS

Closed-Loop CMOS Synchronous Buck Converter | *Virtuoso, Spectre, UMC 180 nm*

Feb – Aug 2026

- Led a team of four to design a transistor-level, voltage-mode synchronous buck converter (3.3 V to 1.8 V at 100 mA) to a specification from Green PMU Semi.
- Closed the loop with a two-stage error amplifier (about 80 dB DC gain), Type-III compensation, ramp generator, PWM comparator, 10–12 ns non-overlap dead-time generator and tapered gate drivers.
- Spectre transient results: 1.80 V output, 26.7 mV peak-to-peak ripple and 0.75 ms settling at 1 MHz in CCM; 89.3% efficiency calculated from losses.

Two-Stage Op-Amp Design and Layout | *Cadence Virtuoso, Layout XL, UMC 180 nm*

2026

- Designed a two-stage Miller-compensated op-amp (20 μ A bias, 2 pF Miller capacitor), revised from 76 dB to about 80 dB DC gain; used as the converter's error amplifier and PWM comparator.
- Drew the full layout, including the compensation capacitor array; DRC and LVS clean.

Standard-Cell Layout Library | *Virtuoso Layout XL, UMC 180 nm*

Mar – Apr 2026

- Drew INV, NAND2, MUX2, XOR2 and OAI311 cells from transistor schematic to layout, with OAI311 routed in both M1 and M2 variants; all cells DRC and LVS clean.

Smart Agriculture for Hilly Regions | *Smart India Hackathon, semi-finalist*

- Sensor-based canal irrigation for Sikkim terrace farms; solar and LDR sensing automate watering.

PUBLICATIONS

Design and Simulation of a CMOS-Based Synchronous Closed-Loop DC-DC Buck Converter in 180 nm Technology

U. Gupta, S. Dollin, G. VK, A. Hosamani, S. Kotabagi | NKCON, SECAB University

Submitted, 2026

EXPERIENCE & LEADERSHIP

Vice-Chair, IEEE Student Branch

KLE Technological University

Apr 2025 – Present

Hubballi, Karnataka

- Organise workshops, seminars, hackathons and student engagement activities for the branch.

Visteon Scholar Program

Industry Training Program

2025

India

- Completed industry training in embedded systems, networking and automotive technologies.